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EXAMINER

LEE, EUGENE

ART UNIT PAPER NUMBER

2815

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Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 8, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi 5,060,033. Takeuchi discloses (see, for example, Fig. 1h) a MOS transistor (device) comprising an insulating film (gate dielectric) 103, substrate (substrate that has a first conductivity region) 101, gate electrode 105, side wall insulating film (pair of sidewall spacers) 108, and source and drain regions (a pair of silicon or silicon alloy inwardly concaved source/drain region of a second conductivity type formed in said substrate) 106. The source and drain regions are inwardly concaved and bend (inflection points) directly underneath the gate electrode. The channel region (first channel region) directly beneath the gate electrode is larger than the channel region (second channel region) between the inflection points.

Takeuchi does not disclose an inflection point which occurs between 50-250 Å laterally beneath said gate electrode and at a depth of between 25-100 Å beneath said gate dielectric. However, the depth of the source/drain junctions and the distance between the inflection point and the gate electrode and gate dielectric are result effective variables that one of ordinary skill in the art would optimize for affecting the channel region in a field effect transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have an inflection point

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which occurs between 50-250 Å laterally beneath said gate electrode and at a depth of between 25-100 Å beneath said gate dielectric, in order to form a channel region, and since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding the limitation “having a concentration of impurities in a range between $1 \times 10^{18} / \text{cm}^3 - 3 \times 10^{21} / \text{cm}^3$ ”, see, for example, column 4, lines 66-67 wherein Takeuchi discloses a range between $1 \times 10^{16} \text{ cm}^{-3}$ to $6 \times 10^{18} \text{ cm}^{-3}$.

Regarding the limitation “recesses, wherein the recesses have an inwardly concaved geometry with inflection points; ... a silicon or silicon alloy layer deposited into the recesses”, this is a product-by-process limitation of forming the source/drain regions, and since the claims are directed towards structure, and Takeuchi structurally discloses source/drain regions, the claims are not structurally distinct from that what is shown in Takeuchi.

Regarding claims 8, and 9, see, for example, column 8, lines 18-21 wherein Takeuchi discloses an n-channel transistor as well as a p-channel transistor.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi ‘033 as applied to claims 1, 8, 9, and 11 above, and further in view of Takeuchi 5,970,351. Takeuchi ‘033 does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi ‘351 discloses (see, for example, FIG. 11 (c)) a MOSFET comprising

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elevated source and drain regions 7B with a facet structure. In column 12, lines 45-63, Takeuchi '351 teaches that such a structure provides reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric in order to reduce parasitic capacitance.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9, and 11 above, and further in view of Choi 6,057,582. Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode in order to reduce hot carrier effects.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi '033 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi 6,057,582. Takeuchi '033 in view of Takeuchi '351 does not disclose a gate dielectric

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layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode in order to reduce hot carrier effects.

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9, and 11 above, and further in view of Choi et al. 5,793,088. Takeuchi does not disclose a pair of deposited silicon or silicon alloy regions having a first conductivity type formed between said pair of deposited silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region. However, Choi discloses (see, for example, FIG. 2 and FIG. 3) a structure 106 comprising halo regions 120, 122. Choi teaches that halo regions provide higher punchthrough voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use halo regions in order to attain a higher punchthrough voltage.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9, and 11 above, and further in view of Hwang 5,567,966. Takeuchi does not disclose a silicide formed on said silicon or silicon alloy source/drain

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regions. However, Hwang discloses (see, for example, Fig. 6) a transistor comprising source and drain regions 24, and TiSi_2 regions (silicide) 20. In column 2, lines 17-19, Hwang teaches reduced source/drain resistance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a silicide formed on said silicon or silicon alloy source/drain regions in order to reduce resistance.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek et al. 6,274,894 B1 in view of Takeuchi 5,970,351. Takeuchi '033 discloses (see, for example, Fig. 1h) a MOS transistor (device) comprising an insulating film (gate dielectric) 103, substrate (first conductivity region of a substrate) 101, gate electrode 105, side wall insulating film (pair of sidewall spacers) 108, and source and drain regions (a pair of silicon or silicon alloy inwardly concaved source/drain region of a second conductivity type formed in said substrate) 106. The source and drain regions are inwardly concaved and bend (inflection points) directly underneath the gate electrode. The channel region directly beneath the gate electrode is larger than the channel region between the inflection points. Takeuchi '033 does not disclose silicon-germanium alloy source/drain regions. However, Wieczorek discloses (see, for example, column 6, lines 8-23) that SiGe (silicon-germanium) in the source/drain regions have a lower bandgap, which lowers contact resistance. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use silicon-germanium alloy in order to lower contact resistance.

Takeuchi '033 in view of Wieczorek does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon

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alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi '351 discloses (see, for example, FIG. 11 (c)) a MOSFET comprising elevated source and drain regions 7B with a facet structure. In column 12, lines 45-63, Takeuchi '351 teaches that such a structure provides reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric in order to reduce parasitic capacitance.

Regarding the limitation "recesses, ... wherein the recesses have an inwardly concaved geometry with inflection points; a silicon-germanium alloy layer deposited into the recesses", this is a product-by-process limitation that discloses a method of forming source/drain regions that are inwardly concave, however, since the claims are directed towards product, such process claims, which do not structurally distinguish the product, are given no patentable weight.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi 5,060,033 in view of Wieczorek et al. '894 B1 in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi 6,057,582. Takeuchi '033 in view of Wieczorek in view of Takeuchi '351 does not disclose a gate dielectric layer being thicker beneath the outside edges of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker

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than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a gate dielectric layer being thicker beneath the outside edges of said gate electrode than the gate dielectric layer beneath the center of said gate electrode in order to reduce hot carrier effects.

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi 5,060,033 in view of Wieczorek et al. 6,274,894 B1. Takeuchi discloses (see, for example, ig. 1h) a MOS transistor (device) comprising an insulating film (gate dielectric) 103, substrate (first conductivity region of a substrate) 101, gate electrode 105, side wall insulating film (pair of sidewall spacers) 108, and source and drain regions (a pair of silicon or silicon alloy inwardly concaved source/drain region of a second conductivity type formed in said substrate) 106. The source and drain regions are inwardly concaved and bend (inflection points) directly underneath the gate electrode. The channel region (first channel region) directly beneath the gate electrode is larger than the channel region (second channel region) between the inflection points. Takeuchi does not disclose silicon-germanium alloy source/drain regions. However, Wieczorek discloses (see, for example, column 6, lines 8-23) that SiGe (silicon-germanium) in the source/drain regions have a lower bandgap, which lowers contact resistance. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use silicon-germanium alloy in order to lower contact resistance.

Regarding the limitation “recesses, wherein the recesses have an inwardly concaved geometry with inflection point; a silicon-germanium alloy layer deposited into

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the recesses”, this is a product-by-process limitation that discloses a method of forming source/drain regions that are inwardly concave, however, since the claims are directed towards product, such process claims, which do not structurally distinguish the product, are given no patentable weight.

OPTIMIZATION OF RANGES

A. Optimization Within Prior Art Conditions or Through Routine Experimentation

Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) (Claimed process which was performed at a temperature between 40°C and 80°C and an acid concentration between 25% and 70% was held to be prima facie obvious over a reference process which differed from the claims only in that the reference process was performed at a temperature of 100°C and an acid concentration of 10%.); >see also *Peterson*, 315 F.3d at 1330, 65 USPQ2d at 1382 (“The normal desire of scientists or artisans to improve upon what is already generally known provides the motivation to determine where in a disclosed set of percentage ranges is the optimum combination of percentages.”); < ** *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969) (Claimed elastomeric polyurethanes which fell within the broad scope of the references were held to be unpatentable thereover because, among other reasons, there was no evidence of the criticality of the claimed ranges of molecular weight or

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molar proportions.). For more recent cases applying this principle, see *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

B. Only Result-Effective Variables Can Be Optimized

A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. In *re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977) (The claimed wastewater treatment device had a tank volume to contractor area of 0.12 gal./sq. ft. The prior art did not recognize that treatment capacity is a function of the tank volume to contractor ratio, and therefore the parameter optimized was not recognized in the art to be a result-effective variable.). See also *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980) (prior art suggested proportional balancing to achieve desired results in the formation of an alloy).

Product-by-Process Limitations

While not objectionable, the Office reminds Applicant that “product by process” limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be

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determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Response to Arguments

11. Applicant's arguments filed 6/12/06 have been fully considered but they are not persuasive.

The new limitations are product-by-process limitations that do not structurally distinguish the source/drain regions formed in Takeuchi from the source/drain regions stated in the applicant's claims. Therefore, Takeuchi still structurally reads on the limitations stated in the applicant's claims.

Regarding the applicant's argument on page 9, fifth paragraph that combining Takeuchi with Choi is impermissible hindsight, this argument is not persuasive. It must be recognized that any judgement on obviousness in any sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the invention was made, and does not include knowledge gleaned only from the Applicant's disclosure, such a reconstruction is proper, *In re McLaughlin*, 443 F. 2nd 1392; 170 USPQ 209 (CCPA 1971).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
August 14, 2006

EUGENE LEE
PRIMARY EXAMINER

A handwritten signature in black ink, appearing to be 'Eugene Lee', written over the printed name and title.